REMARKS

Reconsideration is requested in view of the above amendments and the following remarks. Claim 1 has been revised to include the feature of previous claim 2. Claim 5 has been revised to include the feature of previous claim 6. Support for the revisions can be found in, for example, Fig. 4. Claims 2-4 and 6 have been canceled without prejudice. Claims 1 and 5 remain pending in the application. We note that claims 1-6 are not listed in the "pending" box 4 of the Summary Sheet.

Claim Rejections – 35 USC § 102

Claims 1 and 2 are rejected under 35 USC § 102(b) as being anticipated by Ishikura et al. (US 2002/0079556). Applicant respectfully traverses this rejection. Claim 1 has been revised to include the feature of previous claim 2. Claim 2 has been canceled without prejudice. Applicant is not conceding the correctness of the rejection.

Claim 1 requires a dummy diffused region provided between an area under a dummy layer part and one of a digital circuit part and a analog circuit part. Claim 1 also requires a power-supply potential applied to the dummy diffused region.

The present configuration is advantageous in that, for example, most of a collector current, which is represented by "id" in Fig. 4, can be supplied from the dummy diffused region. As a result, the fluctuation of an electric potential of an n-well region in the analog circuit part can be decreased, and consequently a deterioration of circuit properties of the analog circuit part can be suppressed more effectively without increasing the size of the semiconductor integrated circuit device (see page 6, lines 8-18 and 29-33 of the specification and Fig. 4).

Ishikura et al. fail to disclose a dummy diffused region provided between an area under a dummy layer part and one of a digital circuit part and a analog circuit part, as required by claim 1. Nor do Ishikura et al. disclose a power-supply potential applied to the dummy diffused region, as required by claim 1. Instead, Ishikura et al. discuss a semiconductor device including a dummy diffused layer 11 or 11a covered completely by a dummy gate electrode 13 or 13a (see Ishikura et al. Figs. 3B, 4B, 5B). The focus of Ishikura et al. disclosure is to prevent the dummy diffused layer 11 or 11a from being

silicided and thus prevent the formation of a noise propagation path in the dummy diffused layer 11 or 11a (see Ishikura et al., paragraph [0081]).

The rejection relies on the dummy diffused layer 11 or 11a of Ishikura et al. as disclosing the present dummy diffused region. Applicant respectfully contends that the dummy diffused layer 11 or 11a in Ishikura et al. is in fact disposed between STIs (shallow trench isolations), as shown in Figs. 3B, 4B, 5B. The dummy diffused layer 11 or 11a in Ishikura et al. is not located between an area under a dummy layer part and one of a digital circuit part and an analog circuit part as required by claim 1.

The rejection also relies on the dummy gate electrode 13 in Fig. 4B as disclosing a power-supply potential as required by claim 1. Applicant respectfully contends that the dummy gate electrode 13 is merely an electrode or, as discussed in paragraph [0082], a floating node with no fixed potential level, rather than that providing a power-supply potential as required by claim 1. The present power-supply potential is distinct from the no fixed potential provided by the dummy gate electrode 13 in Ishikura et al.

The present dummy diffused region is distinct from the dummy diffused layer 11 or 11a of Ishikura et al. also in that the dummy diffused layer 11 or 11a of Ishikura et al. is disposed under the dummy gate electrode 13 or 13a (see Ishikura et al., Figs. 3B, 4B, 5B), and thereby the layout of the dummy diffused layers is limited by the layout of the dummy gate electrodes. As a result, unlike the advantage of avoiding the increase of the semiconductor device size enjoyed by the present invention of claim 1, the capability for reducing the size of the Ishikura et al. semiconductor device is substantially limited.

For at least these reasons, claim 1 is patentable over Ishikura et al.

Claim Rejections – 35 USC § 103

Claims 3 and 5 are rejected under 35 USC 103(a) as being unpatentable over the prior art admitted by Hasegawa (US 5,900,927) in view of Ishikura et al. Applicant respectfully traverses this rejection. Claim 3 has been canceled without prejudice, rendering the rejection moot as to claim 3. Claim 5 has been revised to include the feature of previous claim 6.

Claim 5 requires a dummy diffused region provided between an area under a dummy layer part and one of a digital circuit part and a analog circuit part. Claim 5 also requires a power-supply potential applied to the dummy diffused region. Claim 5 is patentable over the prior art admitted by Hasegawa in view of Ishikura et al. for reasons similar to those discussed above regarding claim 1. The prior art admitted by Hasegawa does not remedy the deficiencies of Ishikura et al. In addition, the rejection states that the recitation "camera" in line 1 of claim 5 would not be given patentable weight since the recitation occurs in the preamble. Applicant respectfully contends that the recitation "camera" has clear significance and should be given patentable weight because the body of claim 5 sets forth structural features of a "camera". Applicant is not conceding the relevance of the rejection to the remaining features of the rejected claim.

Claim 4 is rejected under 35 USC 103(a) as being unpatentable over Hasegawa's admitted prior art in view of Hasegawa. Applicant respectfully traverses this rejection. In view of the dependence of claim 4 on claim 3, Applicant assumes that the rejection intended to include Ishikura et al. as one of the references. Claim 4 has been canceled without prejudice, rendering the rejection moot. Applicant is not conceding the correctness of the rejection.

Claim 6 is listed as rejected on the Summary Sheet, but not rejected in the detailed action. Applicant assumed that claim 6 was to be rejected with claim 5. The feature of claim 6 has been included in claim 5. Claim 6 has been canceled without prejudice. Applicant is not conceding the correctness of the rejection.

In view of the above, favorable reconsideration in the form of a notice of allowance is respectfully requested. Any questions regarding this communication can be directed to the undersigned attorney, Douglas P. Mueller, Reg. No. 30,300, at (612) 455-3804.

Respectfully submitted,

HAMRE, SCHUMANN, MUELLER & LARSON, P.C.
P.O. Box 2902-0902
Minneapolis, MN 55402-0902
(612) 455-3800

Dated: June 21, 2007

By: _____
Douglas P. Mueller
Reg. No. 30,300

DPM/cy